B18 Cont'd.

Fig. 10, 1 pixel of data may also be processed in the operation blocks. --

Please replace the paragraph beginning at line 4 of page 55 with the following rewritten paragraph:

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-- Also, in the above embodiments, as shown in Fig. 2, an example was given of using the DDA data S11 in which the val data was added as valid instruction data to the data (z, R, G, B, α, s, t, q) to be image processed. However, the (z, R, G, B, α, s, t, q) data and the val data may be handled as separate independent data. --

IN THE CLAIMS:

Please amend claims 1 to 7, 9 to 12, 14, 16, 18, 21 to 23, 25, 27, 28, 31, 32, 35, 37, 39 and 40 as follows (all of the pending claims are reproduced below in their entirety for the Examiner's convenience):

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1. (Amended) An image processing apparatus comprising:

a plurality of pixel processing circuits, each provided for processing each of a plurality of pixel data to be processed simultaneously, for processing a plurality of input pixel data in parallel; and

a control circuit for stopping the operation of at least one of said pixel processing circuits when the processing of said pixel data to be processed in the pixel processing circuit is not needed.

2. (Amended) An image processing apparatus as set forth in claim 1, wherein:

said pixel processing circuits operate on the basis of a clock signal; and

said control circuit supplies said pixel processing circuits with said clock signal when judging the pixel processing is needed and stops the supply of said clock signal to said at least one of said pixel processing circuits when judging the pixel processing is not needed.

3. (Amended) An image processing apparatus as set forth in claim 2, wherein each of said pixel processing circuits comprises a plurality of processing circuits connected in series to form a pipeline circuit.

4. (Amended) An image processing apparatus as set forth in claim 3, wherein each of said plurality of processing circuits connected in series within said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control pipeline processing within the pixel processing circuit and the supply of said clock signal.

5. (Amended) An image processing apparatus as set forth in claim 1, wherein

each of said pixel processing circuits performs processing with respect to pixel data of red (R), green (G), and blue (B) of a pixel.

6. (Amended) An image processing apparatus for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing apparatus comprising:

a pixel position judging circuit for judging whether or not a corresponding pixel is positioned within said graphic unit for each of the plurality of pixel data to be processed simultaneously;

a plurality of pixel processing circuits for processing a plurality of pixel data to be processed simultaneously mutually in parallel; and

a control circuit for stopping the operation of the pixel processing circuits other than processing circuits for processing pixel data of pixels positioned within the graphic unit to be processed among said plurality of pixel processing circuits on the basis of the results of the judgement of said pixel position judging circuit.

7. (Amended) An image processing apparatus as set forth in claim 6, wherein:

each of said pixel processing circuits operates on the basis of a clock signal; and

said control circuit supplies said clock signal to pixel processing circuits processing the pixel data of pixels positioned inside the graphic unit to be processed, and stops the supply of said clock signal to pixel processing circuits processing the pixel data of pixels not positioned inside the graphic unit to be processed.

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8. (Unchanged) An image processing apparatus as set forth in claim 7, wherein each of said pixel processing circuits comprises a plurality of processing circuits connected in series so as to perform pipeline processing.

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9. (Amended) An image processing apparatus as set forth in claim 8, wherein each of said plurality of processing circuits connected in series within each said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

10. (Amended) An image processing apparatus as set forth in claim 6, wherein:

said pixel position judging circuit adds validity data indicating the result of the judgement to pixel data processed by said pixel processing circuits; and

said control circuit judges based on the validity data whether to stop the operation of said pixel processing circuits.

11. (Amended) An image processing apparatus comprising:

a plurality of pixel processing circuits, provided for a plurality of pixels to be processed simultaneously, for blending a plurality of first pixel data and a corresponding plurality of second pixel data by blending ratios indicated by a blending ratio data set for each pixel to produce a plurality of third pixel data; and

a control circuit for judging whether or not said pixel processing circuits will perform said blending and stopping the operation of said pixel processing circuits when judging that said blending will not be performed.

12. (Amended) An image processing apparatus as set forth in claim 11, wherein:

each of said pixel processing circuits operates on the basis of a clock signal; and

said control circuit supplies each respective pixel processing circuit with said clock signal when judging that said pixel processing circuit will perform blending and stops the supply of said clock signal to said pixel processing circuit when judging that it will not perform said blending.

13. (Unchanged) An image processing apparatus as set forth in claim 12,

wherein each of said pixel processing circuits comprises a plurality of processing circuits connected in series so as to perform pipeline processing.

14. (Amended) An image processing apparatus as set forth in claim 13, wherein each of said plurality of processing circuits connected in series within each said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

15. (Unchanged) An image processing apparatus as set forth in claim 11, further comprising a storage circuit for storing said second pixel data, wherein said control circuit rewrites the second pixel data stored in said storage circuit by said first pixel data when judging that blending will not be performed and rewrites the second pixel data stored in the storage circuit by said third pixel data when judging that blending will be performed.

16. (Amended) An image processing apparatus for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the basis of the same processing conditions, and using as valid data the results of the

processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing apparatus comprising:

a plurality of image processing circuits, provided for a plurality of pixels to be processed simultaneously, for blending a plurality of first pixel data and a corresponding plurality of second pixel data by a blending ratio indicated by a blending ratio data set for each pixel to produce a plurality of third pixel data; and

a control circuit for judging whether or not a corresponding pixel is positioned within said graphic unit to be processed for each of said plurality of pixels to be processed simultaneously and stopping the operation of a pixel processing circuit when judging that said corresponding pixel is not positioned within said graphic unit or when judging that said blending will not be performed on the basis of said blending ratio data.

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17. (Unchanged) An image processing apparatus comprising:

a storage circuit;

a plurality of pixel processing circuits, provided for a plurality of pixels to be processed simultaneously, for producing a plurality of second pixel data from a plurality of first pixel data;

a comparing circuit for comparing a plurality of first depth data of said plurality of first pixel data and a plurality of second depth data of a plurality of third pixel data stored

in said storage circuit in correspondence with said plurality of first depth data; and

a control circuit for judging whether or not to rewrite third pixel data corresponding to second depth data stored in said storage circuit by second pixel data and stopping the operation of the corresponding pixel processing circuit when judging not to rewrite.

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18. (Amended) An image processing apparatus as set forth in claim 17, wherein:

said pixel processing circuit operates on the basis of a clock signal; and

said control circuit supplies said pixel processing circuit with said clock signal when judging to rewrite the third pixel data stored in the storage circuit with the second pixel data and stopping the supply of said clock signal to the pixel processing circuit when judging not to rewrite the third pixel data stored in the storage circuit by the second pixel data.

19. (Unchanged) An image processing apparatus as set forth in claim 18, wherein each of said pixel processing circuits comprises a plurality of processing circuits connected in series so as to perform pipeline processing.

20. (Unchanged) An image processing apparatus as set forth in claim 19, wherein each of said plurality of processing circuits connected in series within said pixel

processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

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21. (Amended) An image processing apparatus for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing apparatus comprising:

a storage circuit;

a plurality of pixel processing circuits, provided for a plurality of pixels to be processed simultaneously, for producing a plurality of second pixel data from a plurality of first pixel data;

a comparing circuit for comparing a plurality of first depth data of said plurality of first pixel data and a plurality of second depth data of a plurality of third pixel data stored in said storage circuit in correspondence with said plurality of first depth data; and

a control circuit for judging whether or not a corresponding pixel is positioned within said graphic unit to be processed for each of said plurality of pixels to be

processed simultaneously, judging whether or not to rewrite said third pixel data corresponding to said second depth data stored in said storage circuit with said second pixel data on the basis of the result of the comparison, and stopping the operation of at least one of said pixel processing circuits when judging that the corresponding pixel is not positioned within said graphic unit or when judging not to rewrite.

22. (Amended) An image processing method for performing image processing by using pixel processing circuits, each provided for each of a plurality of pixels to be processed simultaneously, for processing a plurality of input pixel data in parallel, comprising the steps of:

judging whether or not on the basis of said pixel data the pixel processing of said processing circuits is needed; and

stopping operation of at least one of said pixel processing circuits when judging the pixel processing of said at least one processing circuit is not needed.

23. (Amended) An image processing method as set forth in claim 22, further comprising the steps of:

supplying said pixel processing circuit with a clock signal when judging the pixel processing is needed; and

stopping the supply of said clock signal to said pixel processing circuit when

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judging the pixel processing is not needed.

24. (Unchanged) An image processing method as set forth in claim 23, wherein each of said pixel processing circuits performs pipeline processing by a plurality of processing circuits connected in series.

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25. (Amended) An image processing method as set forth in claim 24, wherein each of said plurality of processing circuits connected in series within each of said pixel processing circuits has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

26. (Unchanged) An image processing method as set forth in claim 22, wherein said pixel processing is processing with respect to pixel data for deciding output of red (R), green (G), and blue (B) of a pixel.

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27. (Amended) An image processing method for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the basis of the same processing conditions, and using as valid data the results of the

processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing method comprising the steps of:

judging whether or not a corresponding pixel is positioned within said graphic unit to be processed for each of the plurality of pixel data to be processed simultaneously;

processing a plurality of pixel data to be processed simultaneously mutually in parallel in a plurality of pixel processing circuits; and

stopping the operation of the pixel processing circuits other than processing circuits for processing pixel data of pixels positioned within the graphic unit to be processed among said plurality of pixel processing circuits on the basis of the results of the judgement.

28. (Amended) An image processing method as set forth in claim 27, further comprising the steps of:

supplying a clock signal to the pixel processing circuits processing the pixel data of pixels positioned inside the graphic unit to be processed; and

stopping the supply of said clock signal to pixel processing circuits processing the pixel data of pixels not positioned inside the graphic unit to be processed.

29. (Unchanged) An image processing method as set forth in claim 28, wherein

each of said pixel processing circuits performs pipeline processing by a plurality of processing circuits connected in series.

30. (Unchanged) An image processing method as set forth in claim 29, wherein each of said plurality of processing circuits connected in series within said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

31. (Amended) An image processing method comprising the steps of:

using a plurality of pixel processing circuits provided for a plurality of pixels to be processed simultaneously to blend a plurality of first pixel data and a plurality of second pixel data by blending ratios indicated by a blending ratio data set for each pixel to produce a plurality of third pixel data;

judging based on said blending ratio data whether to perform said blending by said pixel processing circuits; and

stopping the operation of at least one of said pixel processing circuits when judging that said at least one pixel processing circuit will not perform said blending.

32. (Amended) An image processing method as set forth in claim 31, further

comprising the steps of:

supplying a corresponding pixel processing circuit with a clock signal when judging that said corresponding pixel processing circuit will perform blending; and

stopping the supply of said clock signal to at least one of said pixel processing circuits when judging that said at least one pixel processing circuit will not perform said blending.

33. (Unchanged) An image processing method as set forth in claim 32, wherein each of said pixel processing circuits performs pipeline processing by a plurality of processing circuits connected in series.

34. (Unchanged) An image processing method as set forth in claim 33, wherein each of said plurality of processing circuits connected in series within said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

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35. (Amended) An image processing method for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the

basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing method comprising the steps of:

using a plurality of image processing circuits, provided for a plurality of pixels to be processed simultaneously, to blend a plurality of first pixel data and a plurality of second pixel data by a blending ratio indicated by a blending ratio data set for each pixel to produce a plurality of third pixel data;

judging whether or not a corresponding pixel is positioned within a corresponding one of said graphic units for each of said plurality of pixels to be processed simultaneously; and

stopping the operation of at least one of said pixel processing circuits when judging that the corresponding pixel is not positioned within said graphic unit to be processed or when judging that said blending will not be performed on the basis of said blending ratio data.

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36. (Unchanged) An image processing method comprising the steps of:

using a plurality of pixel processing circuits, provided for a plurality of pixels to be processed simultaneously, to produce a plurality of second pixel data from a plurality of first pixel data;

comparing a plurality of first depth data of said plurality of first pixel data and a plurality of second depth data of a plurality of third pixel data stored in a storage circuit in correspondence with said plurality of first depth data; and

judging whether or not to rewrite third pixel data corresponding to second depth data stored in said storage circuit by second pixel data and stopping the operation of the corresponding pixel processing circuit when judging not to rewrite.

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37. (Amended) An image processing method as set forth in claim 36, further comprising the steps of:

supplying said pixel processing circuit with a clock signal when judging to rewrite the third pixel data stored in the storage circuit with the second pixel data; and

stopping the supply of said clock signal to the pixel processing circuit when judging not to rewrite the third pixel data stored in the storage circuit by the second pixel data.

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38. (Unchanged) An image processing method as set forth in claim 37, wherein each of said pixel processing circuits performs pipeline processing by a plurality of processing circuits connected in series.

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39. (Amended) An image processing method as set forth in claim 38, wherein

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each of said plurality of processing circuits connected in series within said pixel processing circuit has a flag storage portion, said flag storage portions of said plurality of processing circuits are connected in series to constitute a shift register, and said shift register is used to control said pipeline processing and the supply of said clock signal.

40. (Amended) An image processing method for expressing an image to be displayed on a display means by a composite of graphic units of a predetermined shape, processing pixel data of a plurality of pixels positioned within each graphic unit on the basis of the same processing conditions, and using as valid data the results of the processing of the pixel data of the pixels positioned within said graphic unit to be processed among pixel data of a plurality of pixels to be processed simultaneously, said image processing method comprising the steps of:

using a plurality of pixel processing circuits, provided for a plurality of pixels to be processed simultaneously, to produce a plurality of second pixel data from a plurality of first pixel data;

comparing a plurality of said first depth data of said plurality of first pixel data and a plurality of second depth data of a plurality of third pixel data stored in a storage circuit in correspondence with said plurality of first depth data;

judging whether or not a corresponding pixel is positioned within said graphic unit to be processed for each of said plurality of pixels to be processed simultaneously,